

Bitland Electronics Co.,LTD

Board name: Mother Board Schematic

Project name: BM5XXX

Version: REV:1.X

initial Date: 201X-0X-XX

New update:

1. System Block Diagram & Schematic page description;

2. Power Block Diagram & Discription;

3. Annotations & information;

4. Schematic modify Item and history;

5. Power on & off Sequence;

6. ACPI Mode Switch Timings;

7. Power On Sequence Map;

8. CLOCK Distribution;

9. Power Distribution;

Bitland Confidential

Hardware drawing by:


Hardware check by:

EMI Check by:

Power drawing by:

Power check by:

Manager Sign by:

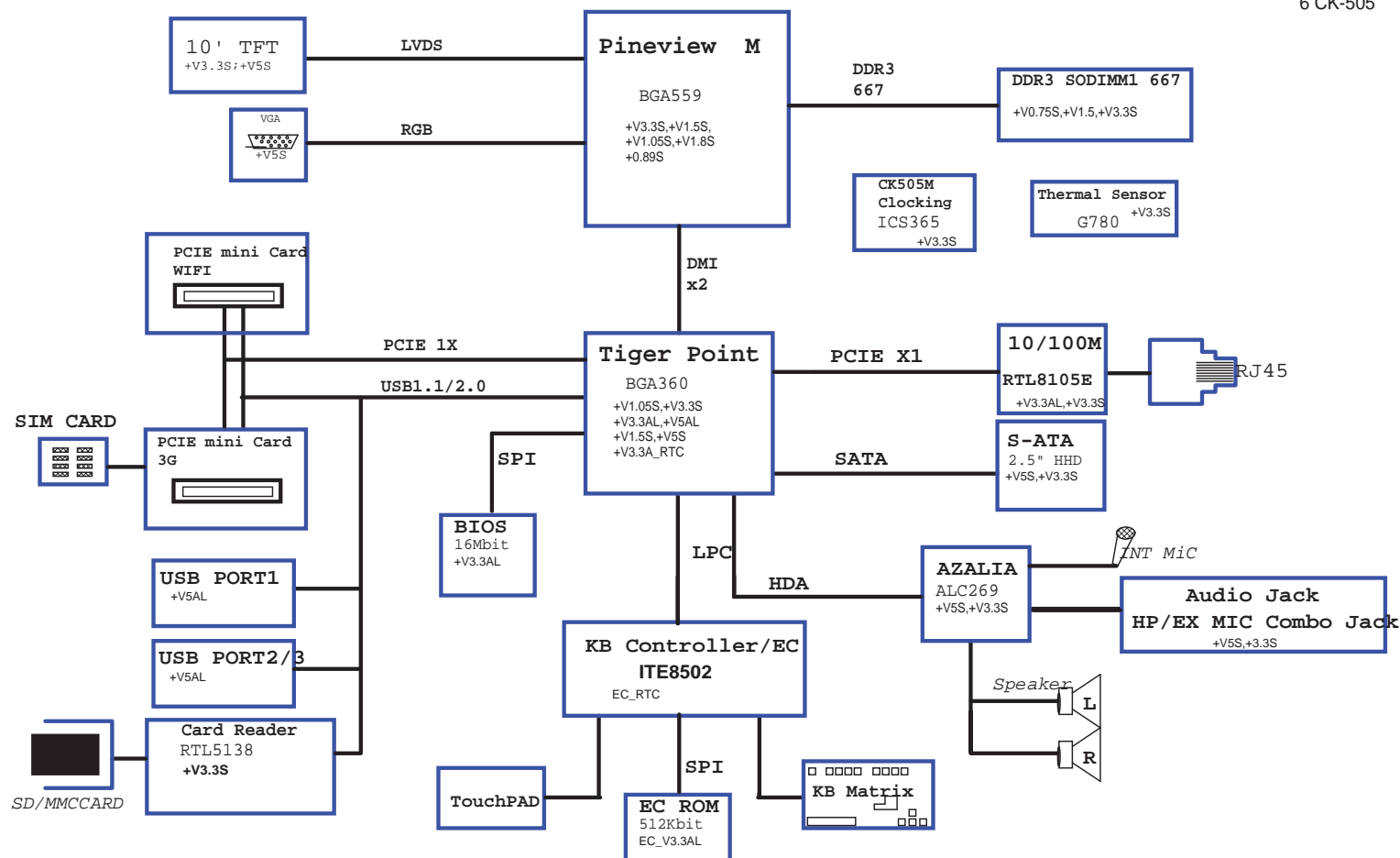
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Page Name		Title	
Size A3	Project Name BM5080	Rev 1.2	
Date:		Sheet 1 of 42	
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SYSTEM BLOCK Ver:C

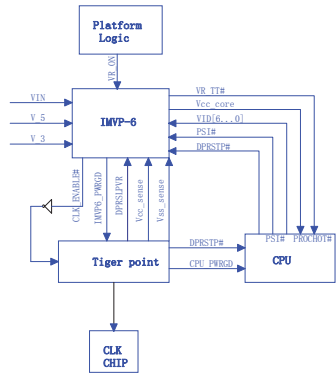
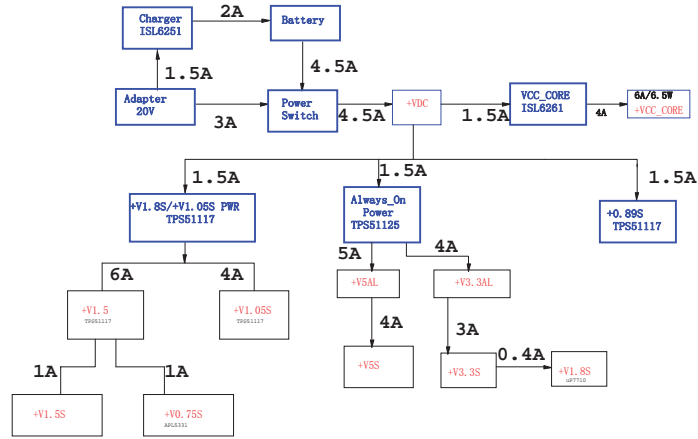
CONTENT

- 1 Title
- 2 System Block & Index
- 3 PWR Block & description
- 4 NOTE
- 5 Sch Modify and history
- 6 CK-505

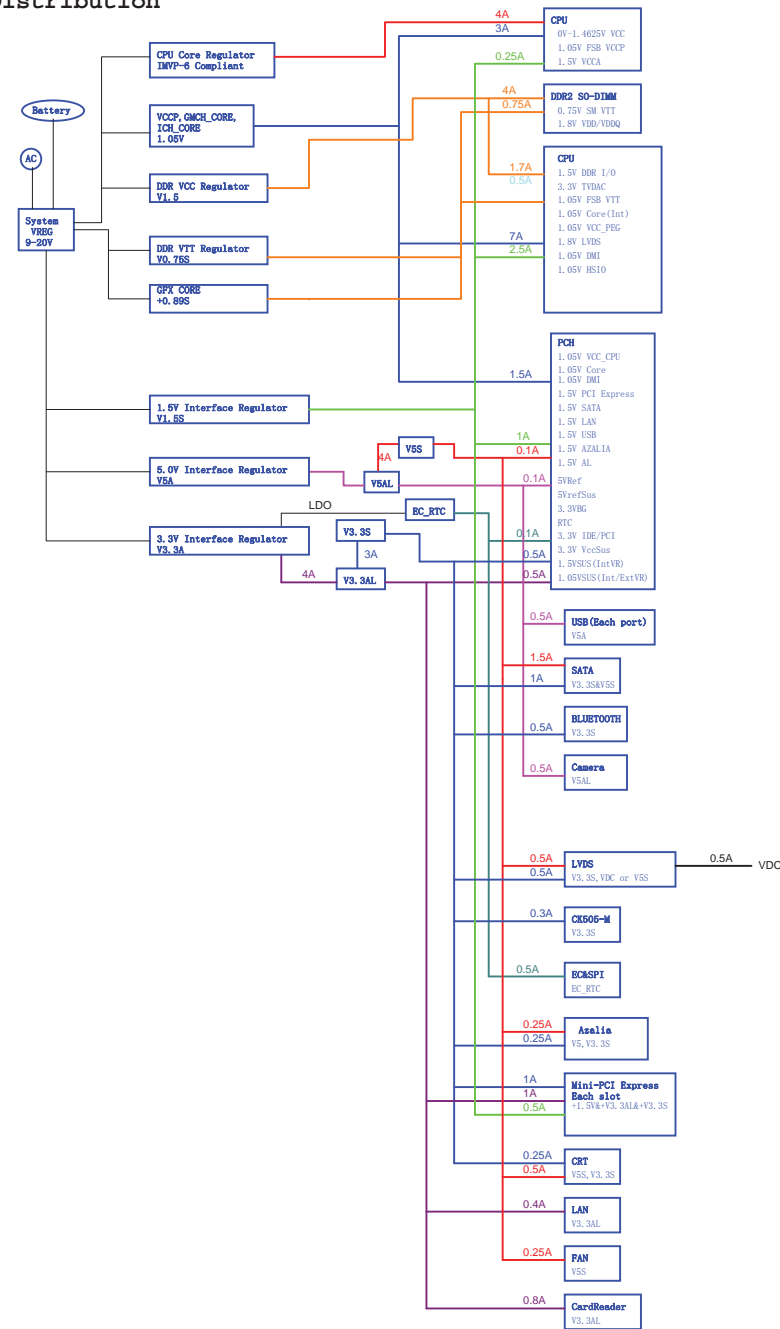


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S18 POWER BLOCK Ver:A



POWER Distribution



Voltage Rails

+VDC	Primary DC system power supply (9V-20V)
+VBATTERY	Battery Power supply (9-20V)
+VCC_CORE	Core Voltage for CPU
+V1.05S	1.05V for Pineview & Tiger point core / FSB VTT
+V1.5	1.5V power rail for DDR3
+V0.75S	0.75V DDR3 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail
+V0.89S	0.89V for GFX

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%
Top(Signal1)	
Power	
Ground	
Bottom(Signal4)	

USB Table

USB Port#	Function Description
0	
1	
2	
3	
4	
5	
6	
7	

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

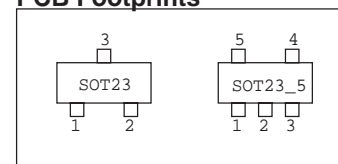
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events


LID switch from EC
Power switch from EC

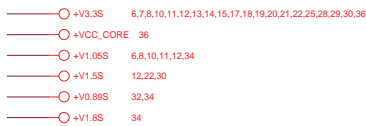
PCB Footprints



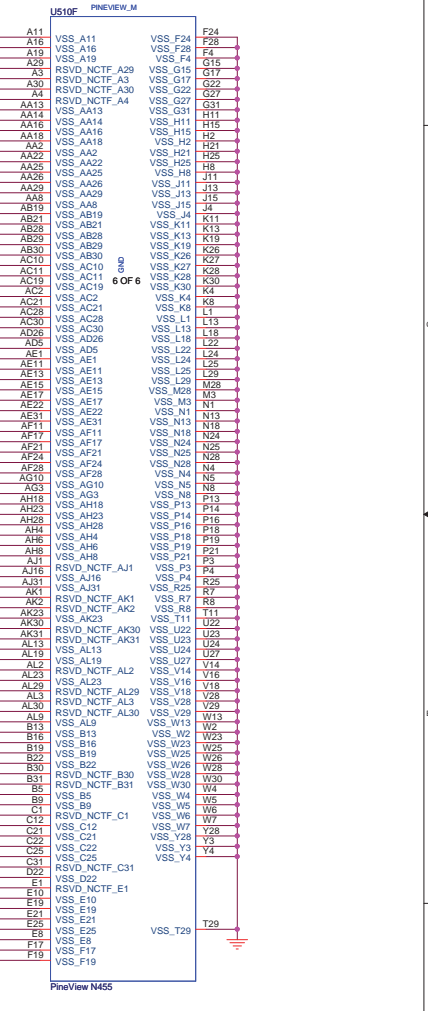
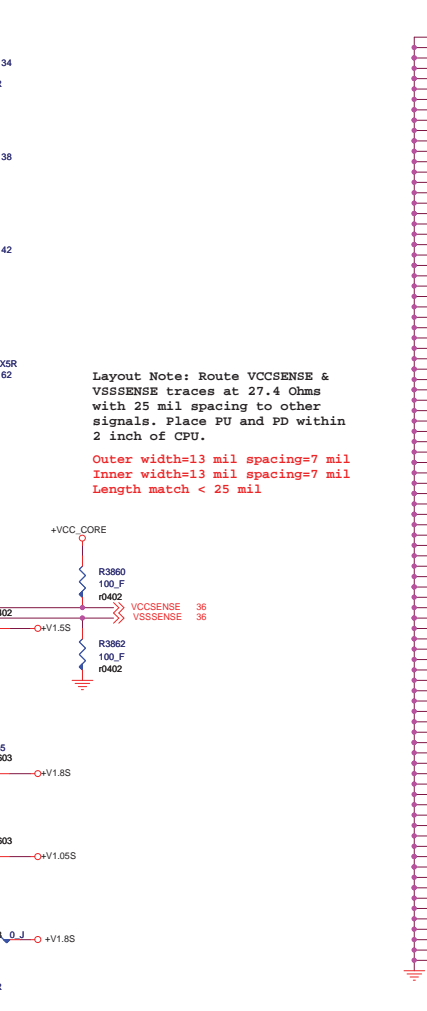
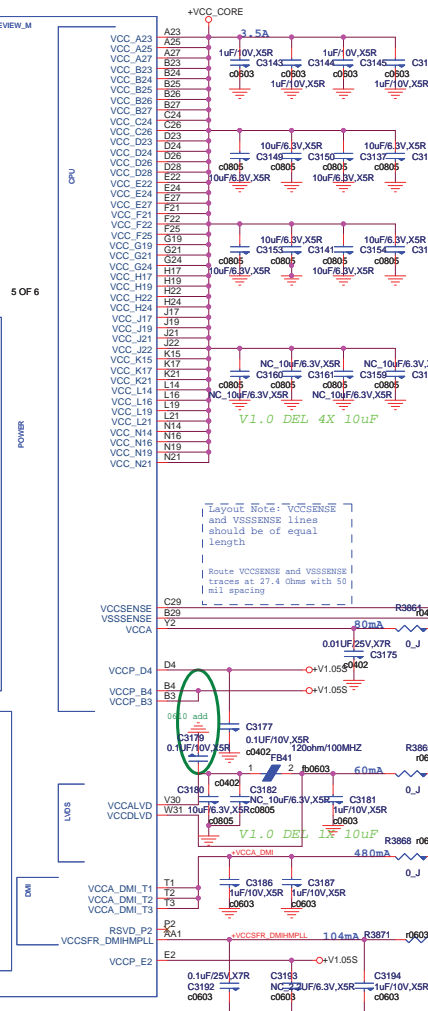
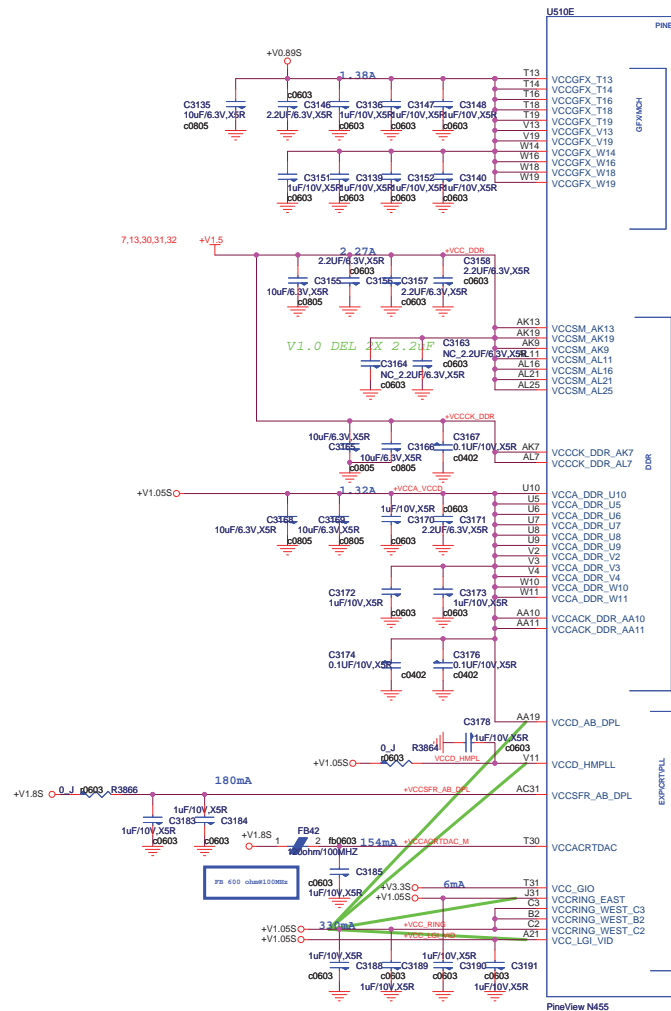
ns: Component marked "ns" is not stuff

Schematic modify Item and history:

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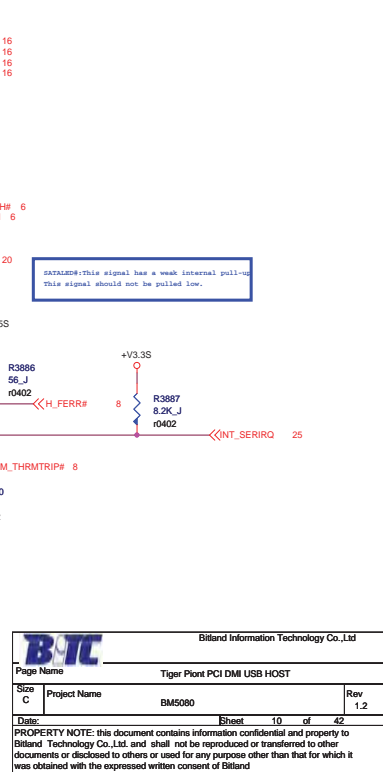
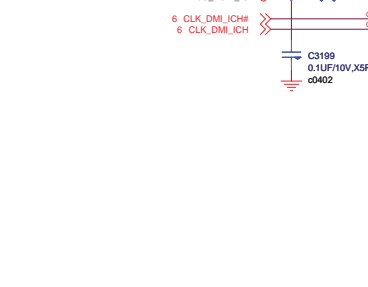
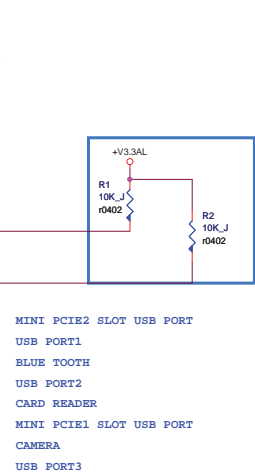
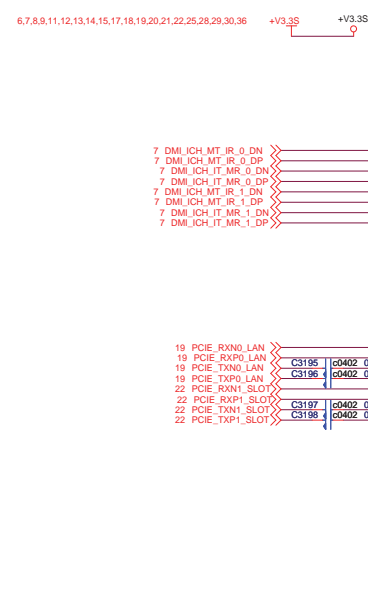


6,7,8,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36 +V3.3S +V3.3S

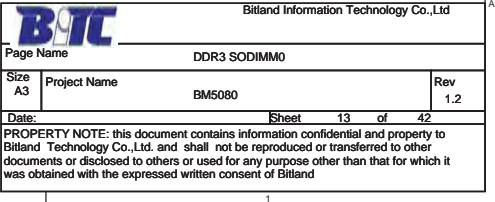


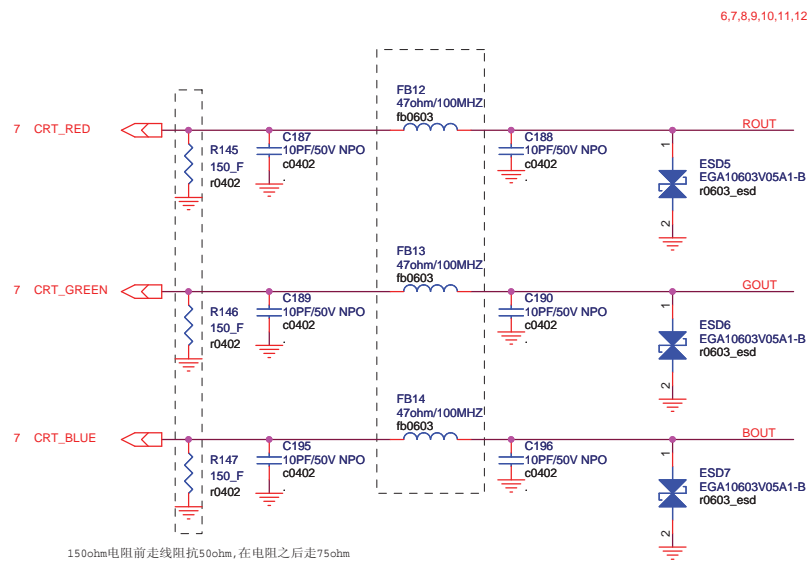
Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.
Outer width=13 mil spacing=7 mil
Inner width=13 mil spacing=7 mil
Length match < 25 mil

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing

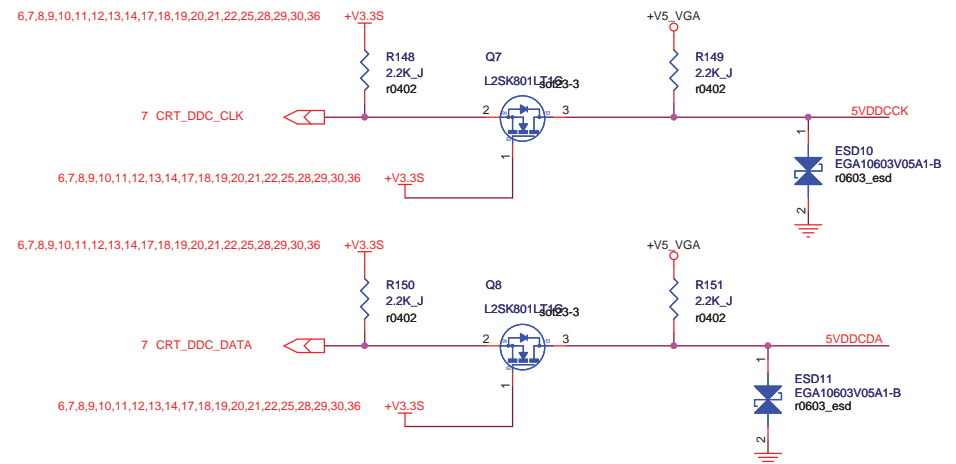
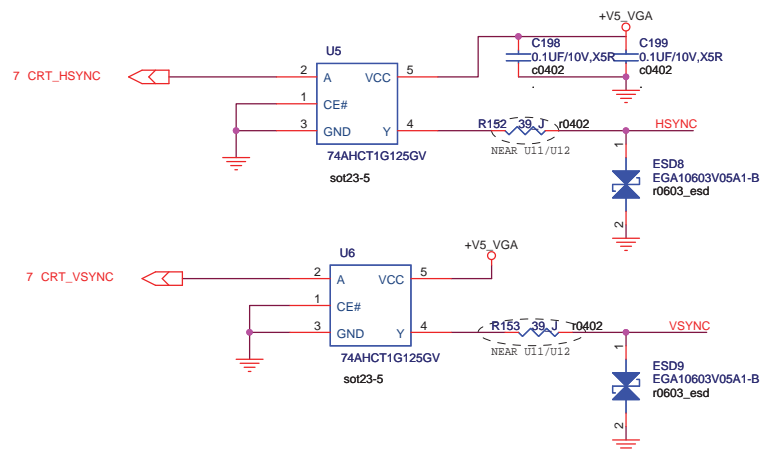
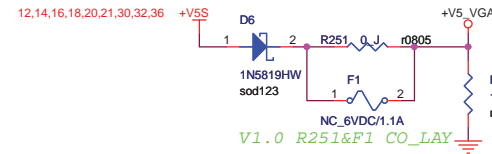
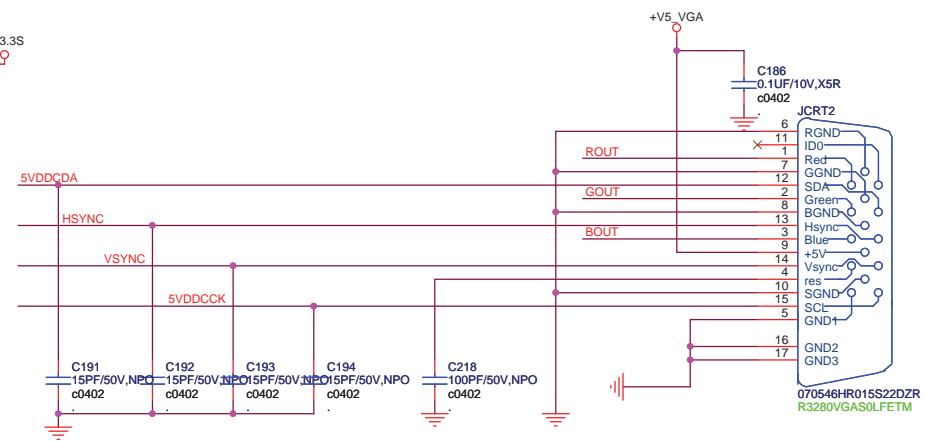




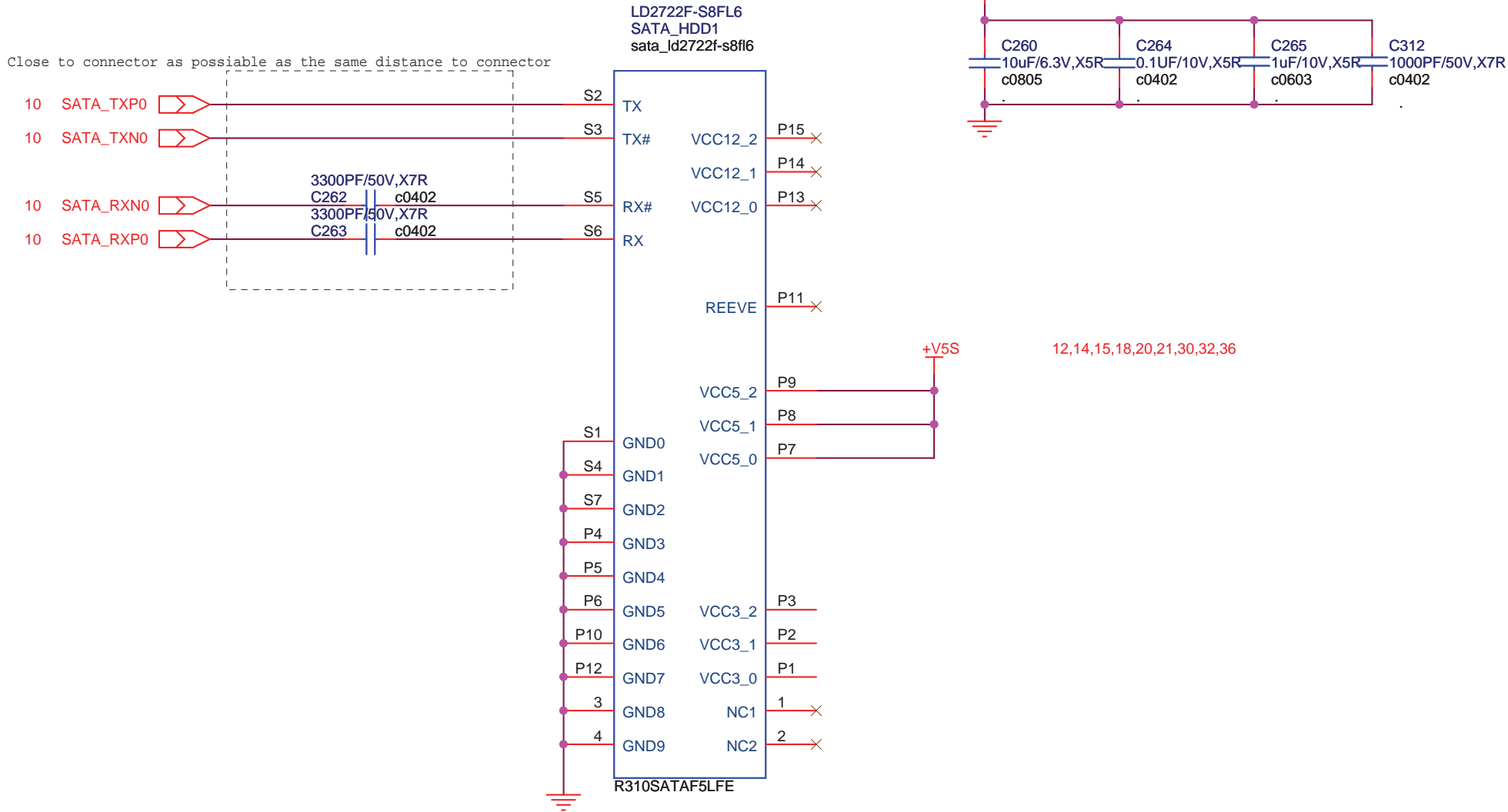




V1.1 20101203: SI
C188 C190, C196, C189, C195. C187 10pF



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Rev

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ID

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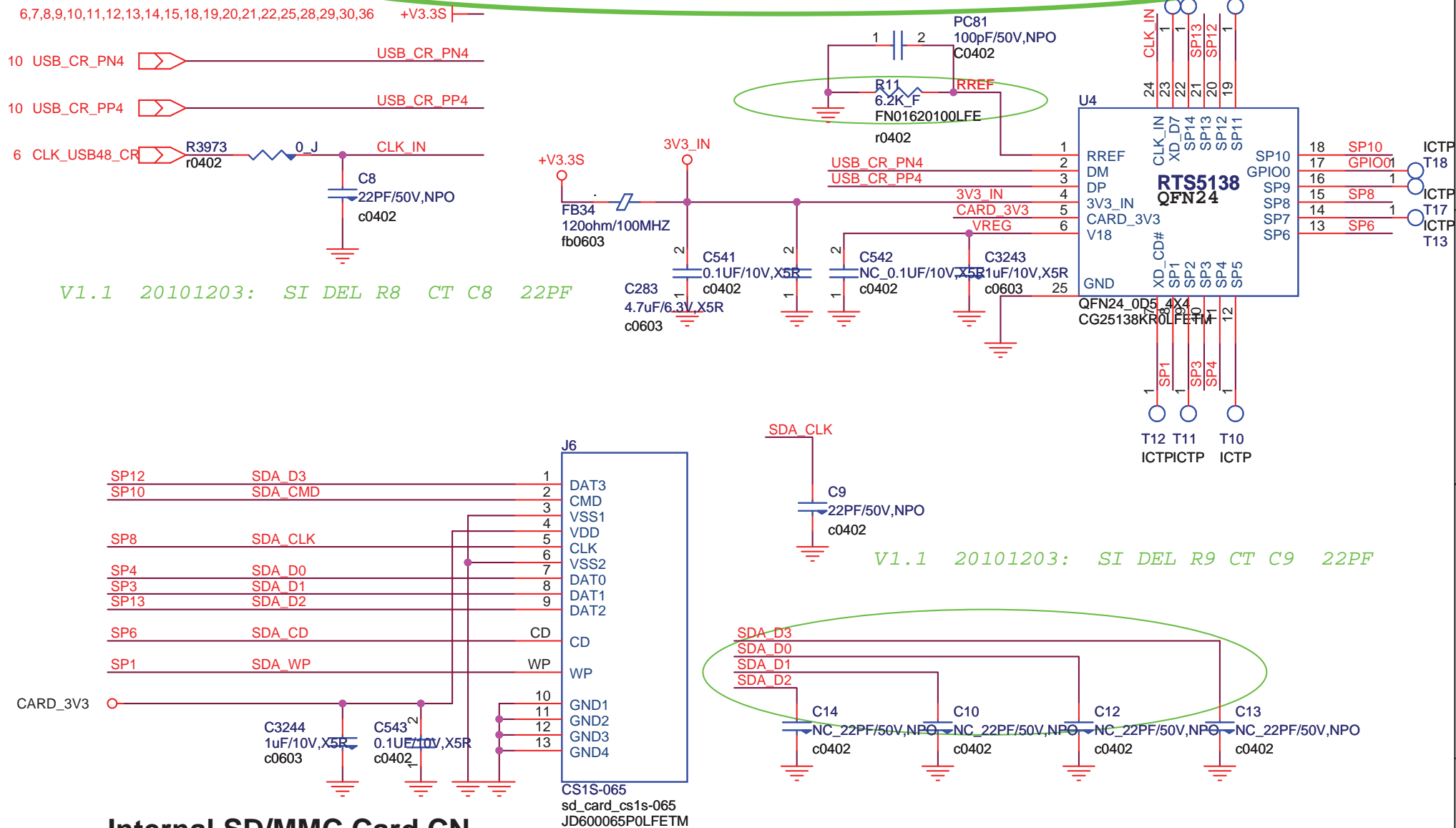
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REV1.2 R11 's Footprint change 0603 to 0402



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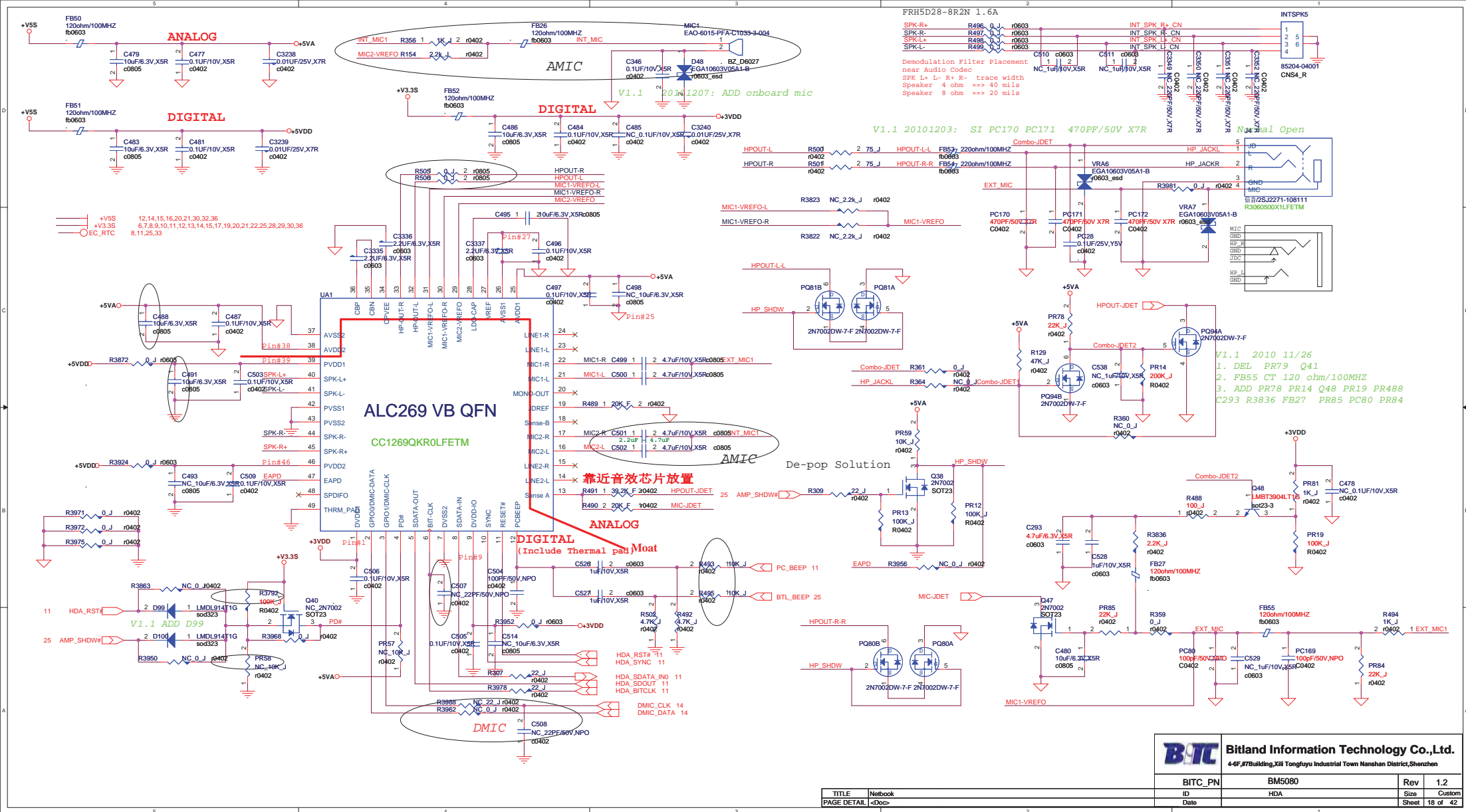
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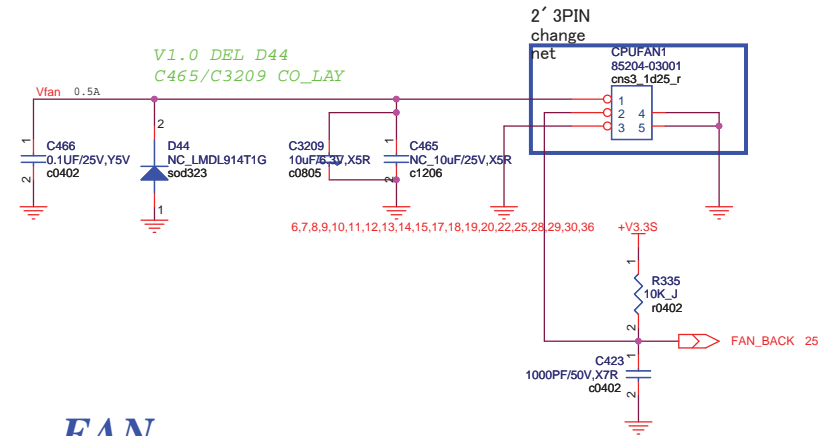
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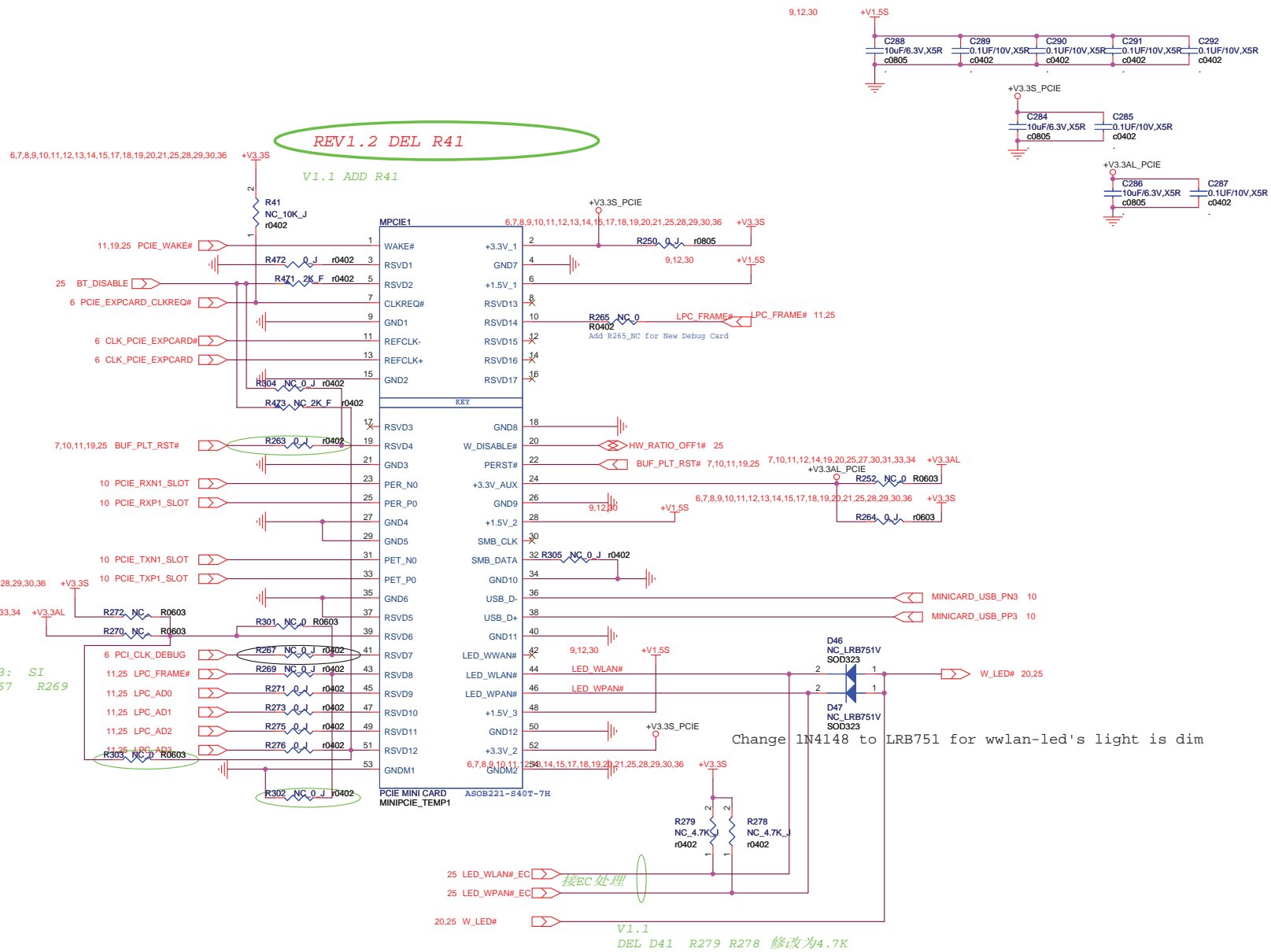




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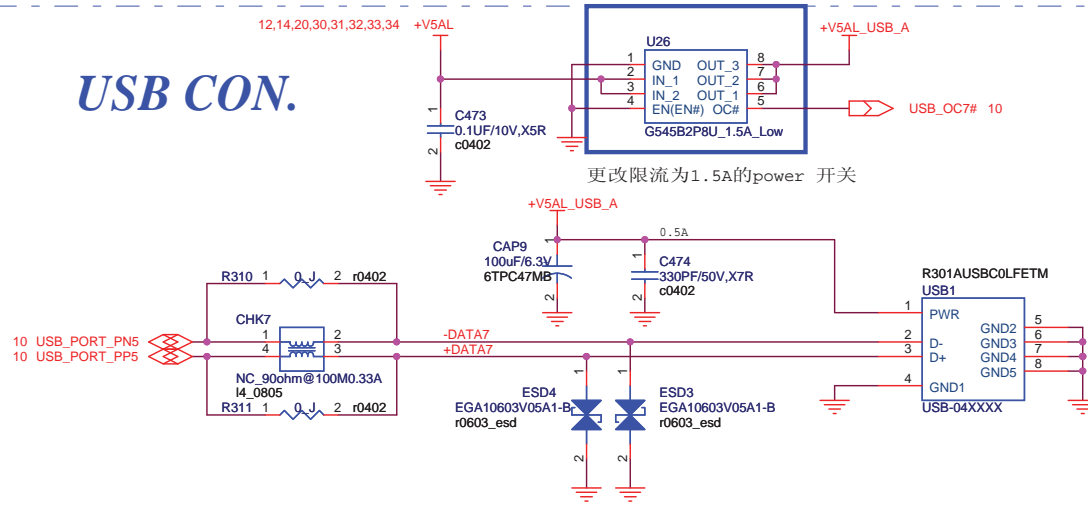


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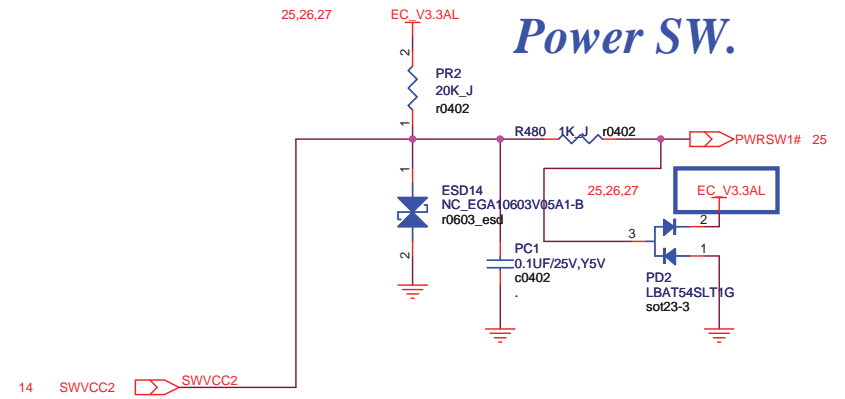


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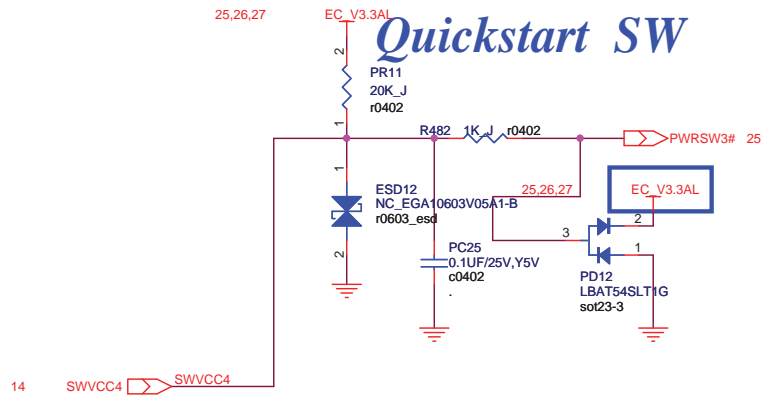
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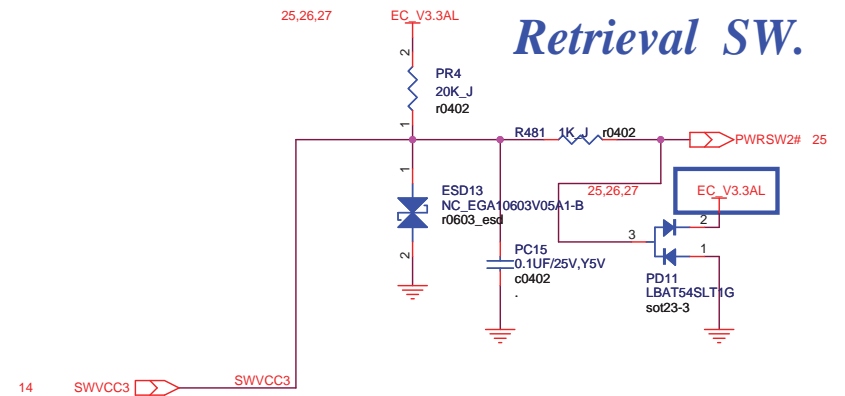
Power SW.



Quickstart SW



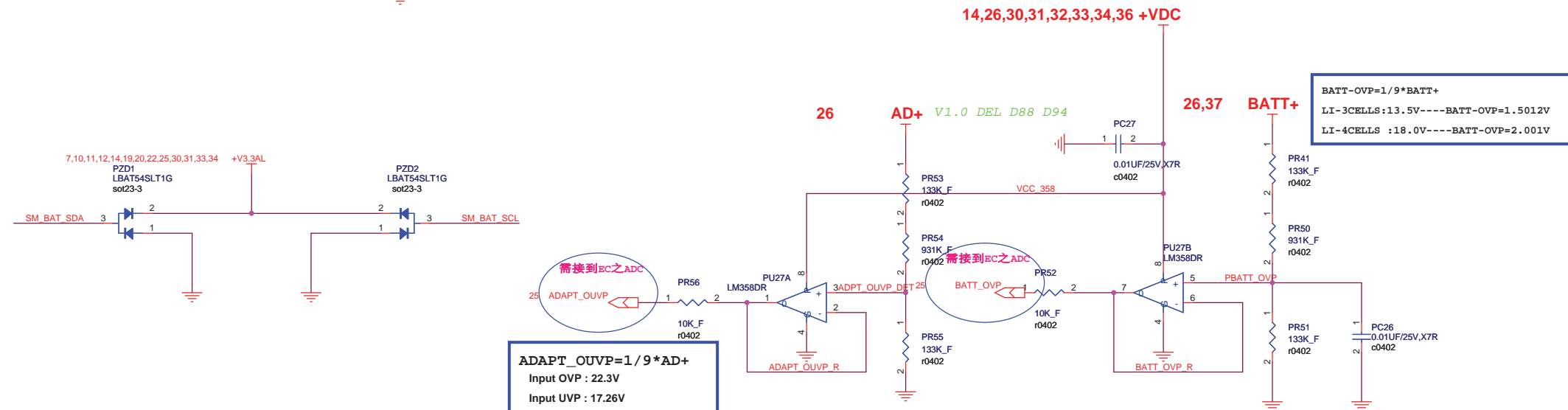
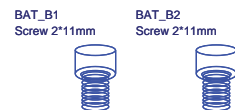
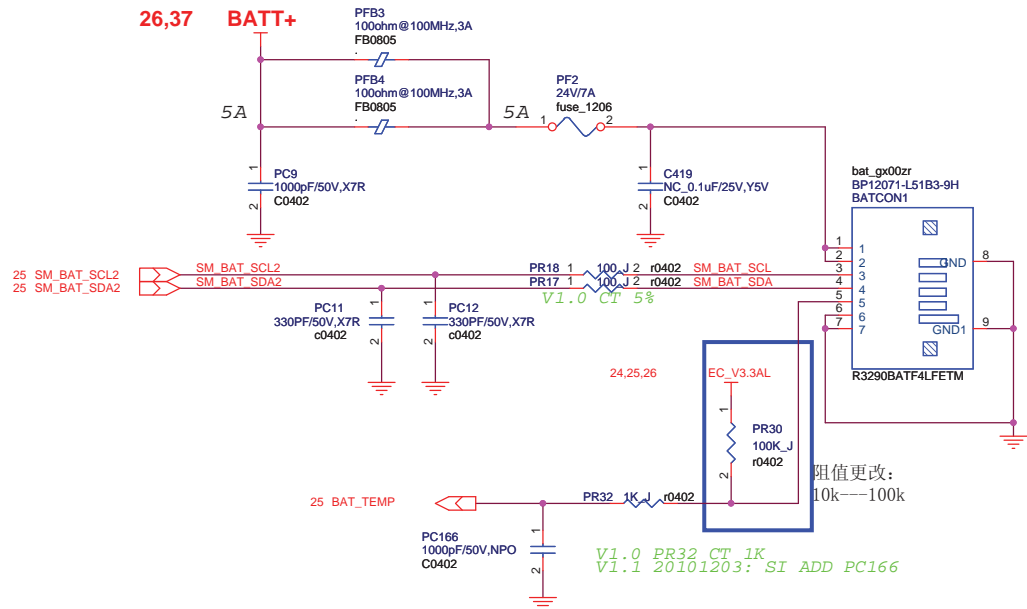
Retrieval SW.




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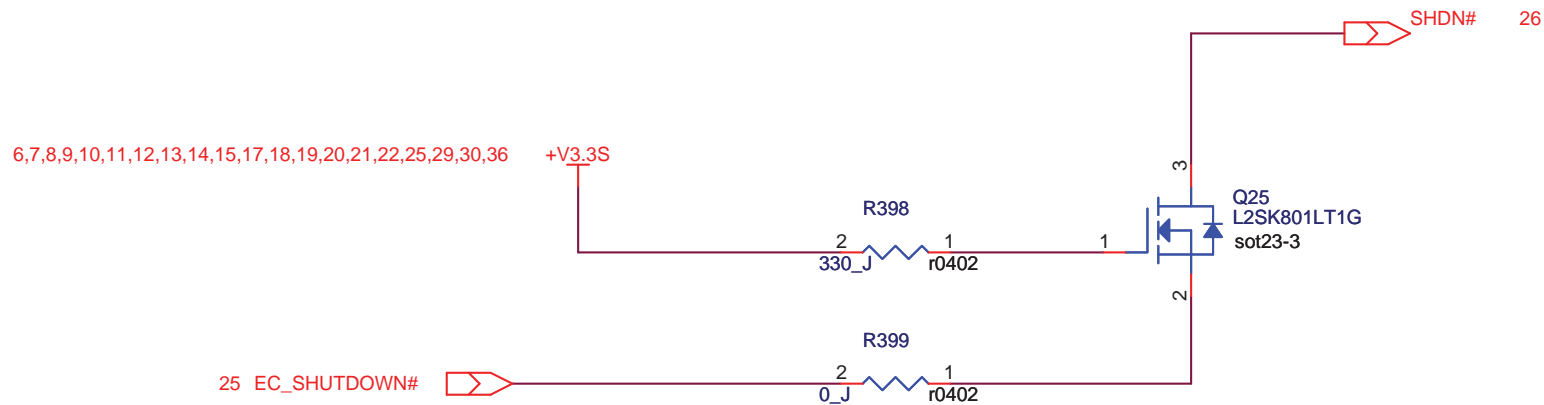
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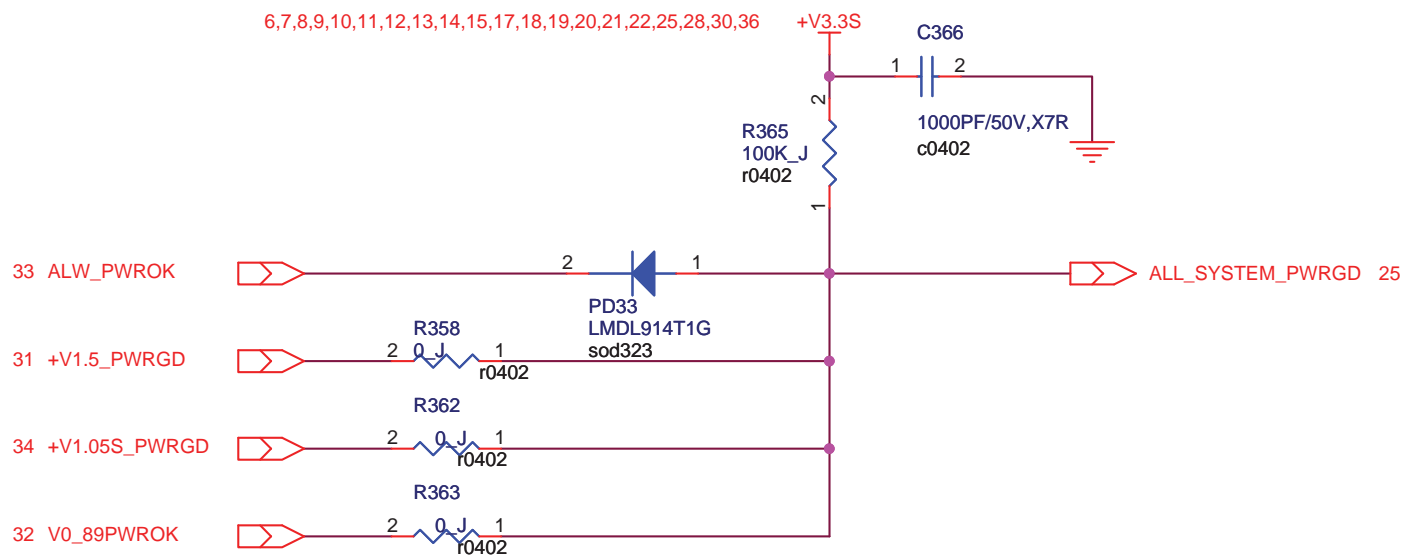
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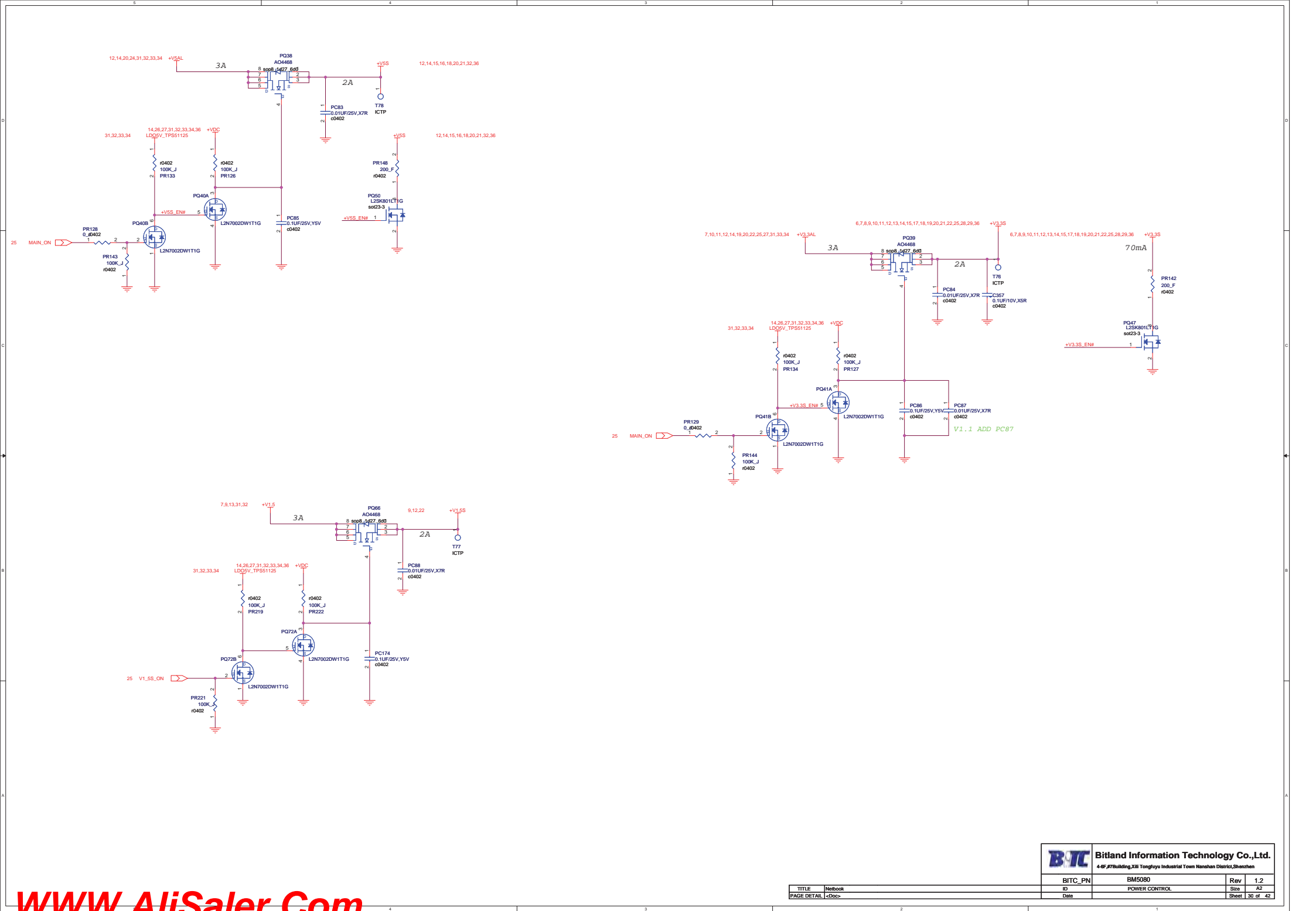
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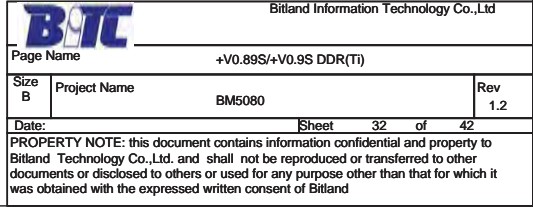
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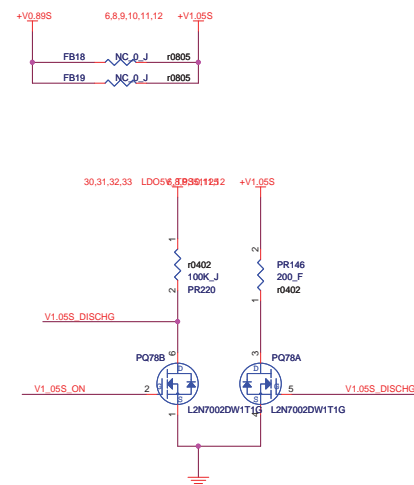
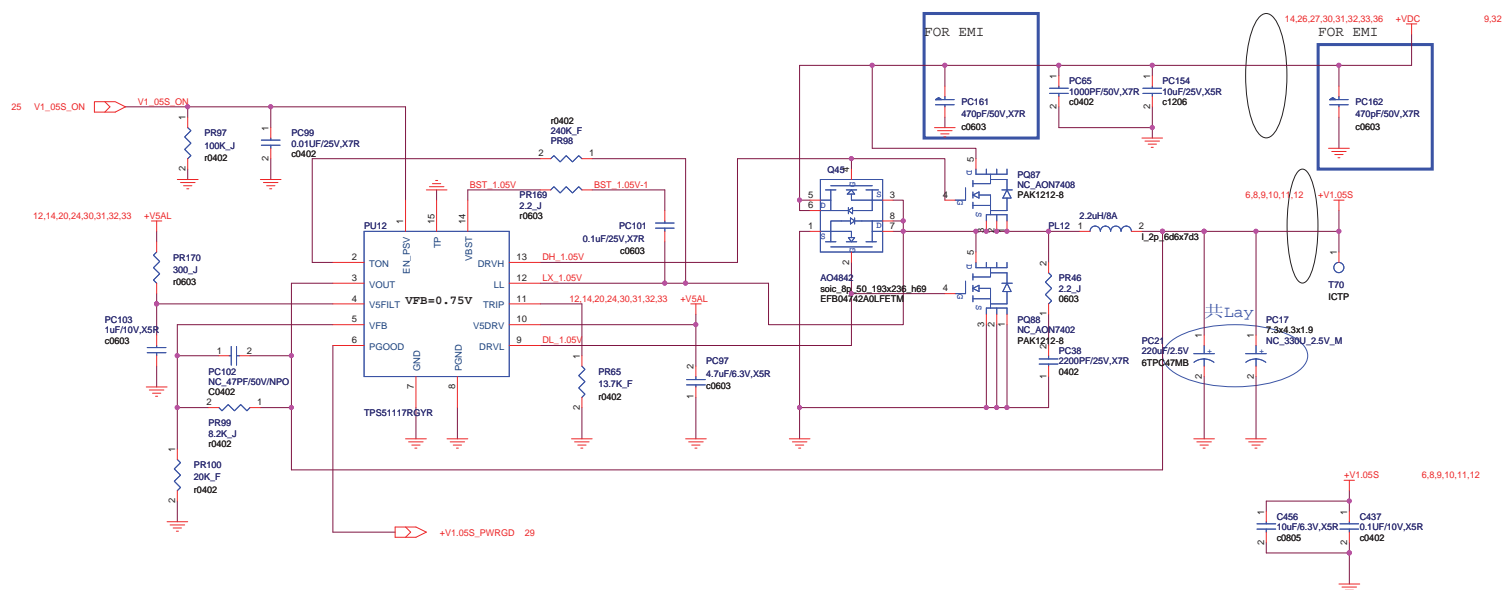
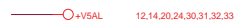


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D

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C

C

B

E

A

A



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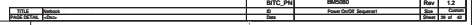
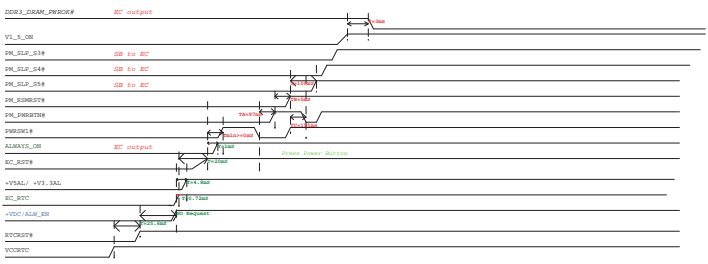
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- 20101126_____V1.1
1. Page6 ADD R3773 R3774 R3772
 2. Page11 ADD R42
 3. Page14 DEL Q9 R155 R156 PC172
 4. Page18 ADD D99
 5. Page18 Modify Codec Combo Jack circuit
 6. Page 22 ADD R41
 7. Page 28 ADD PC87
 8. Page14 移动 C346 D48到LVDS CN附近

- 20110124_____V1.2
1. Page 6 R3766 CT 10 OHM.
Page 6 DEL R3772 R3774
 2. Page14 Del C347 D49
 3. Page17 change R11\Footprint from 0603 to 0402 。
 4. DEL ALL Power Jumpers
 5. Page25 LPC 通道上预留56PF电容位置
 6. Page19 DEL R477 R478 R479
增加 C38 位置0603 0 OHM电阻
增加 LD1
 7. Page11 DEL R42
 8. Page22 DEL R41

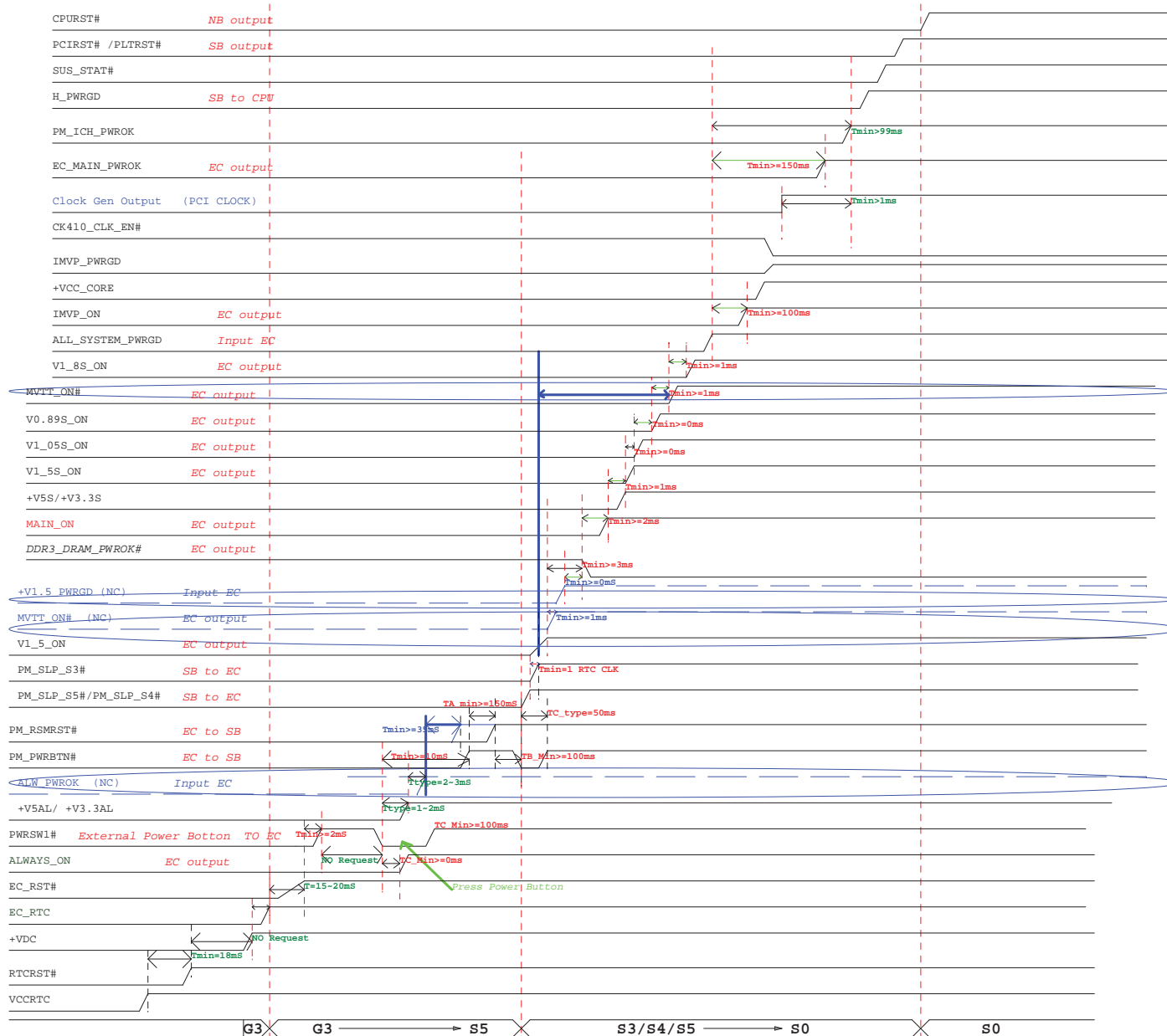
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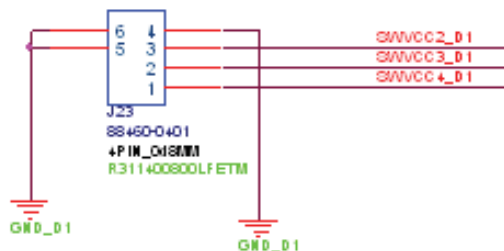
BM5XXX Power On/Off Sequence Specification(Battery Mode)



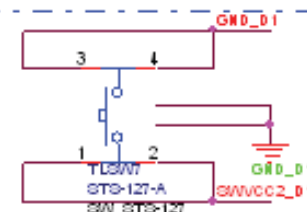
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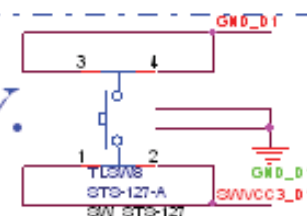
onboard stereo microphone



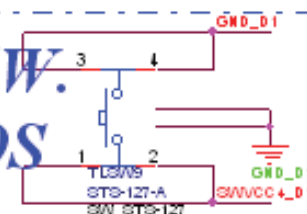
Power SW.



Retrieval SW.



Quickstart SW.
For Meego OS



Power Switch DB



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DB LED/MIC

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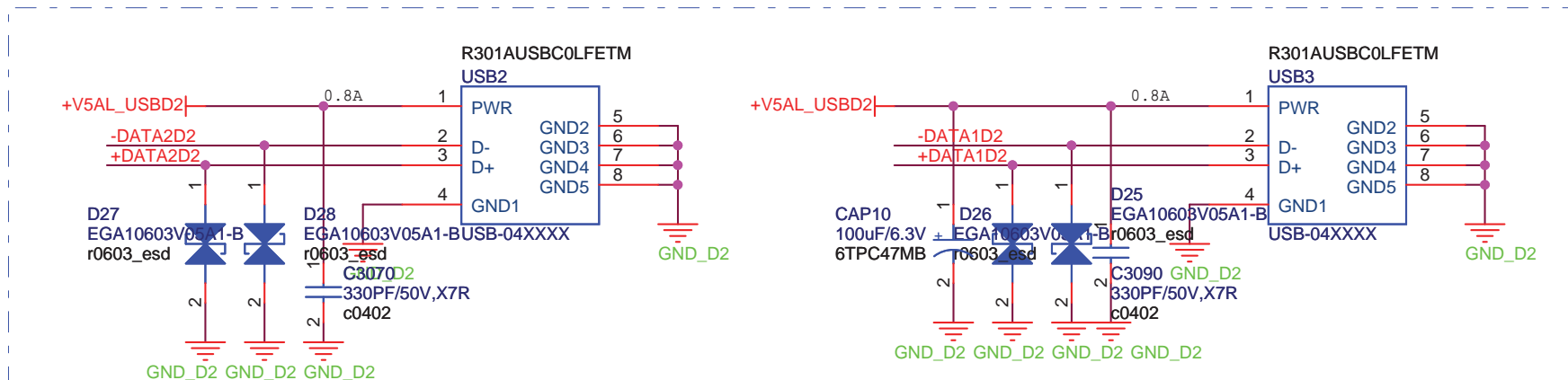
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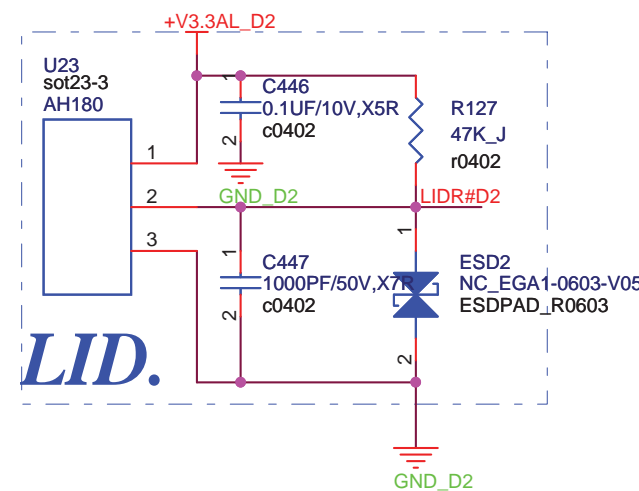
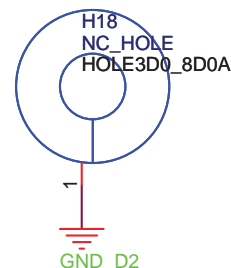
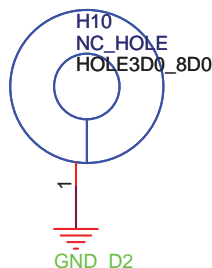
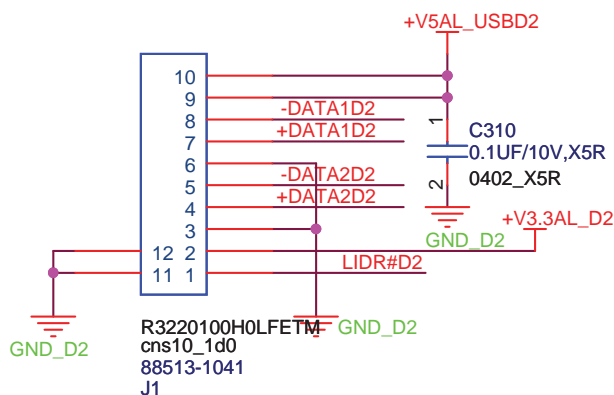
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确认异面FPC排线连接J1顺序OK



USB/LID DB



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DB USB/WL-SW

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